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10/613,006	07/07/2003	Scot A. Kellar	219.40603VX1	4498

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/613,006	KELLAR ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2, 7, 9, 10,14,16-18,21* is/are rejected.

7)☒ Claim(s) *3-6,8,11-13,15,19,20 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/3/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The replacement drawings were received on 1/24/05. These drawings are approved by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 7, 9, 14, 16, and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,724,084 to Hikita et al.

Regarding claims 1, 9, and 16, Hikita discloses a wafer bonding method having the steps of: forming a first wafer ('bottom' 80 in figures 4a, 4b) and a second wafer ('top' wafer in figures 4a, 4b), each including one or more integrated circuit devices (column 9, line 55 – column 11, line 15), metallic lines (88) deposited via an interlevel dielectric (84, 85; figures 1A-1E), and at least one barrier line (87) deposited on an outer edge of the surface (figures 3-4); wherein the metallic lines and the barrier line deposited on the surface of the second wafer are selectively aligned to the first wafer (column 11, lines 1-24), bonded with the lines on the surface of the first wafer (figures 3, 4) to establish electrical connections between active IC devices and form a barrier structure (column 11, lines 9-15; figures 3-4).

Regarding claims 7, 14, and 21, Hikita discloses that the wafers correspond to a single die (figures 4a, 4b), and the barrier structure is formed by one line deposited on the outer edge of the bonded die (figures 4a, 4b). Since the barrier is a metal layer provided enclosing the outer periphery of the bonded dice, it inherently protects them from corrosion, contamination, and crack propagation.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 10, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita et al. in view of U.S. Patent No. 6,340,608 to Chooi et al.

Hikita discloses bonding pads (88) deposited on opposing surfaces of the adjacent wafers to serve as electrical contacts between active IC devices on both the adjacent wafers (see column 9, line 55 – column 11, line 15; figures 1-4), and that the bond pads and barrier lines are formed of the same material (see figures 1-2).

Hikita fails to specify that the bond pads are made of copper.

Chooi teaches that copper interconnection pads for flip chip bonding are advantageous over other connection joints (see column 1, lines 5-18, column 3, lines 1-10, and column 4, lines 1-13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Hikita, such that the bonding pads and barrier are formed of copper, as suggested by Chooi. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use copper as a bond pad/interconnection material, because Chooi shows that it has low inductance, low capacitance, lower cost, and simpler fabrication processes than conventional flip chip bonding pads (Chooi, column 1, lines 5-18; column 3, lines 1-10; column 4, lines 1-13).

Allowable Subject Matter

6. Claims 3-6, 8, 11-13, 15, 19, 20, and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 3, the prior art fails to teach a dielectric recess for ensuring that the metal lines on one wafer contact the metal lines on the other wafer. Instead, the prior, art, such as Hikita, just teaches a visual alignment between the two wafers, and there is no assurance that the metal lines on the two wafers will be aligned or contacted. Since an alignment structure simplifies the alignment and improves the device reliability, the claimed subject matter of claim 3 is considered critical and unobvious.

Regarding claims 4-6, 11-13, 19, and 20, the primary reason for allowability is that the prior art only teaches the usage of a barrier structure as claimed for a single die, and hence, does not suggest applying a barrier to an outer edge of a bonded wafer having a plurality of dice.

Since the prior art of record specifically applies such a barrier to each individual die for either hermetic sealing or stress management of that die, and since a structure having a barrier at the edge of a multi-die wafer does not provide individual sealing for each die, it is the examiner's opinion that the prior art generally teaches away from the claimed feature.

Regarding claims 8, 15, and 22, the prior art generally teaches the usage of a single guard ring deposited on the perimeter of the die, but there is no suggestion or motivation for providing a barrier in the shape of concentric rings. It is the examiner's opinion that a person having ordinary skill in the art would have simply used the single barrier ring taught by the prior art, rather than concentric rings, because the structure is simpler to fabricate.

Response to Arguments

8. Applicant's arguments filed 1/24/05 have been fully considered but they are not persuasive.

The Applicant first argues that Hikita differs from the claimed subject matter, since Hikita teaches the bonding of chips, whereas the claims are drawn to the bonding of wafers.

The Applicant is reminded that "during patent examination, the pending claims must be given their broadest reasonable interpretation consistent with the specification." In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000) and that the "PTO applies to verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in applicant's specification." (See MPEP, §2111). Since "wafer" is at its broadest

defined as "a thin slice of semiconductor material with parallel faces used as the substrate for active solid-state devices in discrete or monolithic integrated circuit form" (see definitions for class 257, active solid state devices) or alternately, "a thin slice of semiconductor used as a base for an electronic component or circuit" (Merriam-Webster, 10th edition, 2000), the base substrate of any chip or die could be considered to be a "wafer."

Furthermore, the specification of the present invention fails to appraise one skilled in the art as to what the term "wafer" is considered to encompass. The following ambiguities as to the intended meaning of the term "wafer" appear in the cited portions of the specification: "Figs. 1A-1B illustrate an example three dimensional (3-D) wafer-to-wafer vertical stack forming a single chip" (page 5); "wafer-to-wafer vertical stack of a single chip (individual die)" (page 6); "Figure 7 illustrates an example individual die pair 610..... the die pair 610 including the bottom wafer 710 and the top wafer 720" (page 12); "the bonded wafers correspond to a single die" (original claims 7, 14, and 21), and text in figure 7 calling each die a "wafer." Based on these statements in the specification, it appears that the Applicant is including chips, dice, and any structure using a semiconductor base material in the term "wafer." Hence, based on the Applicant's specification and the definitions of wafer provided supra, the Examiner still considers the chip structures in Hikita to read on the term "wafer."

The Applicant is reminded that the Examiner had already indicated allowability of claims 4-6, 11-13, 19, and 20, based on further limitations to "wafer" indicating the presence of multiple dice which are subsequently singulated. Hence, the inclusion of verbiage in independent claims 1, 9, and 16 further defining or limiting the claimed "wafer" such that it could not be considered to encompass chips and dice would overcome the rejections based on Hikita.

Regarding the combination of Hikita and Chooi, the Applicant further argues that Chooi teaches that it is not desirable to use copper interconnection pads, and that Chooi teaches the use of a photosensitive resin instead.

This is not persuasive, for several reasons. Chooi does teach that the interconnection pads and lines should be and are formed of copper throughout the specification for the same reasons generally known and established in the art, such as low inductance, capacitance, and fabrication complexity (see Chooi, column 1, lines 5-18; column 3, lines 1-10; column 4, lines 1-13). The 'photosensitive resin' used between the copper pads for bonding is a conductive copper photosensitive resin (see Chooi, column 3, lines 20-25). Hence, it is also considered to be copper. Since Chooi shows that copper-copper metal bonds are widely known and used in flip chip bonding, and since Chooi further addresses prior art problems with the copper-copper bonds by using a copper resin, and since the Applicant does not provide any unexpected results obtained by the use of copper or any results in any way deviating from the advantages of copper wiring lines and bond pads widely known in the art, it is the Examiner's opinion that a person skilled in the art would have found it reasonable or desirable to use copper bonds in Hikita based on the teachings of Chooi.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

CRAIG A. THOMPSON
PRIMARY EXAMINER